Nowadays multiprocessor computer systems are used in various fields of science and technology and also in industry and economics. At the same time real performance of multiprocessor systems, which are oriented on traditional methods of organization of parallel calculations, often does not exceed 10÷15% from the declared peak one, because it is necessary to realize a number of interprocessor exchange and memory access procedures, and besides that to synchronize sequential processes realized in processors of the system. The main reason of performance reduction is mismatch between “hard” architecture of multiprocessor system and informational structure of wide class of solving tasks.

This problem can be solved with the help of multiprocessor computer systems with “flexible” architecture, which is programmed according to informational structure of the specific task, solving at the moment [1-2]. This concept was implemented due to programmable logic integrated circuits (FPGAs) of high integration used as reconfigurable element base. Computer systems with high “real performance/peak performance” (efficiency) and “real performance/volume” (compact size) ratio can be designed on the basis of FPGAs [3].

Quite a number of reconfigurable computer systems (RCS) experimental models of various configurations based on FPGAs were designed in SRI of multiprocessor computer systems of academician A.V. Kaliaev of Southern Federal University (SRI MCS SFU). The set of experimental models includes both small size single-board devices and systems which consist of thousands processors, and besides, series-produced systems. This fact corroborates theoretical statements of the concept of multiprocessor systems with programmable architecture.

At present in SRI MCS SFU is realized state contract 02.524.12.4002 “Design of family of high-performance multiprocessor computer systems with dynamically rearrangeable architecture on basis of reconfigurable element base and its software for solving tasks of high computational complexity” within federal program “Research and design according to foreground line of development of scientific and technological complex of Russia in 2007-2012”. Within this project has been designed the RCS family:

- computer system of industry level RCS-5 with performance 5 TFlops;
- computer system for corporations or scientific centers RCS-1 with performance 1 TFlops;
- workstation for medium-seized companies RCS-0.2 “Alioth” with performance 200 GFlops;
- accelerators for personal computers RAPC-50 “Phecda” with performance 50 GFlops and RAPC-25 “Merak” with performance 25 GFlops.

The main computational elements of RCS family are basic modules “Alkor” and “Merak”. Circuit boards of these modules were designed with accuracy rating 5 and have 20 conductive layers. Each basic module (BM) contains computational FPGAs, distributed memory, FPGA of basic module controller, FPGAs loading and synchronization subsystems, power and cooling subsystems.
BM “Alkor” is intended to be used as a part of workstation RCS-0.2 “Alioth”, RAPC-50 “Phecda”, and computational blocks RCS-0.2-CB, which are computational nodes of RCS-1 and RCS-5. Computational resource of BM “Alkor” consists of 16 FPGAs Xilinx Virtex-5 xc5vlx110 and 22 memory chips DDRII-800 with total volume of 2816 Mbytes, connected via spatial switching system which provides data exchange between BM components with frequency of 1,2 GHz in every information channel. Performance of BM “Alkor” is 200 GFlops for processing 32-bit data in IEEE-754 format and 50 GFlops for processing 64-bit data in IEEE-754 format.

BM “Merak” is intended to be used as a part of RAPC-25 “Merak”. Computational resource of BM “Alkor” consists of 16 FPGAs Xilinx Spartan-3 xc3s5000 and 26 memory chips DDRII-800 with total volume of 1664 Mbytes, connected via spatial switching system. Performance of BM “Merak” is 100 GFlops for processing 32-bit data in IEEE-754 format and 25 GFlops for processing 64-bit data in IEEE-754 format.

Workstation RCS-0.2 “Alioth” consists of four BM “Alkor”, connected by high-speed LVDS data transfer channels, master controller like IBM PC, basic modules and master controller interface unit, subsystems of power supply, cooling and system status indication. Power consumption of RCS-0.2 during solving tasks does not exceed 1,2 kW.

RAPC-25 and RAPC-50 does not contain master controller. These accelerators consist of one BM and are intended to be used as personal computers accelerators for solving tasks with high computational complexity. The purpose of product design was to create maximum compact, light-weight portable devices which correspond to modern requirements of technical design and ergonomics. Also attention was paid to maximum unification of all these products with the purpose of production cost decreasing. Accelerators may be connected to PC via LVDS data transfer interface and Gigabit Ethernet. Power consumption during solving tasks does not exceed 200 W for RAPC-25 and 300 W for RAPC-50.

Computer system RCS-1 consists of four computational blocks RCS-0.2-CB which are placed into 19” stand Rittal TS-8. Within the stand computational blocks may be connected by LVDS-cables. If RCS-1 is functioning in special accommodations, equipped with air-conditioning system or cooling system, its clock frequency may be increased. In this case performance of computational blocks RCS-0.2-CB may achieve 250 GFlops. As a result performance of RCS-1 may achieve 1 TFlops. At present RCS-1 is functioning in computer centre in SRI MCS SFU.

System RCS-5 may be designed by interconnecting five stands of RCS-1 via Ethernet. At present RCS-5 is assembled in Research Computer Centre of M.V. Lomonosov Moscow State University. During solving tasks of various problem areas RCS-5 provides real performance of 5 TFlops with power consumption of 22 kW.

Software complex, which allows to program designed computer systems of the family, is developed within the state contract. It is known, that creation of configuration files for programming FPGAs is very complicated and requires special knowledge and skills. So the main purpose of development of the software complex for creation applied programs for RCS is significant decreasing of programming time. The main purpose of the software complex is effective realization of computationally complex fragments of tasks from various problem areas on arbitrary hardware resource of computer system.

Software complex of applied programs development contains: assembler Argus v.3.0; high level programming language COLAMO v.2.0; integrated development environment Argus IDE v.3.0 for hardware and software solving of applied tasks; debugger of parallel programs; program interface of access to RCS computational resources; development environment of computational structures Fire!Constructor for scalable parallel-pipeline procedures synthesis; library of circuit designs (IP-cores).
Low level programming language Argus v.3.0 is assembler language, providing low-level access to BM hardware resources. High level language COLAMO is based on implicit description of parallelism and allows to develop effective applied programs for RCS, when information about computer architectural peculiarities is insufficient for developer.

During translation of parallel COLAMO-program translator generates structural component in the form of virtual informational graph of the task. Then, using Fire!Constructor, is established a correspondence between functional elements from IP-cores library and tops of the graph. After that unified computational structure is automatically built according to available hardware resource specified by developer and VHDL-descriptions of computational fragments are formed. Further, using standard CAD software such as Xilinx ISE configuration files for FPGAs are generated.

Program access to basic modules is possible via unified program interface, which allows to use functions of loading/uploading and computations control developed using traditional programming languages (C++, Object Pascal, Java, etc.) with the help of interfaces libraries that can be added to the project.

At the same time with RCS family design, infrastructure of prospective users training is created. Mass access of prospective users to informational resources and software products, designed as a result of the project, will be provided by using global computer network Internet and its services.

References